Naeem Maroof
Curriculum Vitae

PERSONAL DETAILS

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OBJECTIVE STATEMENT

As an accomplished Computer Engineer, I'm driven to ignite innovation in areas of my expertise: Embedded Systems, Low-Power Wireless Connectivity, and Digital Design. My mission is to inspire talent, engineer excellence, and reshape the future.

AREAS OF INTERESTS AND EXPERTISE

- Embedded systems and IoT
- Low power wireless (BLE, Cellular)
- Digital hardware design (Verilog / FPGA)
- Integrated circuit design (Digital/Analog)
- Low power memories and processor design
- Research, development, and technical writing

EDUCATION

Ph.D. Electronics and Communications Engineering `2012-2016`
Hanyang University, South Korea

Studied several course in Digital, Analog, Mixed-signal IC, Reliable Computing, VLSI Design & Test and AI/CV. Worked on different projects in Low power design, Memory design, and Computer vision. Thesis: Robust Low Power CMOS design for Memory & Interface Circuits. Skills: IC Design, VLSI Test, Reliability, Computer Vision

MSc. Electronic Communications and Computer Engineering `2006-2007`
University of Nottingham, United Kingdom

Studied several course in Electronics, Signal Processing, Communications and Computing. Worked on different projects in Design design, Communication systems, RF microelectronics, and Signal processing. Thesis: DSP techniques for enhancement of received GPS signal.

BSc. Computer Engineering `2002-2006`
COMSATS IIT, Pakistan

Studied different course in Electrical/Electronics (circuit analysis and design), Computer (Organization, Architecture, Digital design, Embedded systems and VLSI), Communications, Signal Processing and Computer. Worked on different projects and learnt hardware design, software design, embedded system design, using fpgas and dsp-kits, and analysis of communication systems. Thesis: Implementation of CDMA using TI DSP Kits.

WORK EXPERIENCE

More than 12 years of experience working as full-time employee.

Senior Application Engineer   `09/22-present`

Nordic Semiconductor, Norway, Full-time

> Working as a senior application engineer in RnD department of Nordic Semiconductor, Norway. Involved in technical support related to Nordic specific hardware and software solutions, including SoCs, RTOS, and low power wireless connectivity.

Assistant Professor   `10/18-8/22`

University of Jeddah KSA, Full-time

> Worked as a full time faculty member of Electrical and Electronic Engineering department. Involved in teaching, student support, student advisory, project supervision, curriculum design & review, research work and administration.

Assistant Professor   `9/17-9/18`

KFUEIT Pakistan, Full-time

> Worked as full time member of Computer Engineering department. Major duties included: teaching, student advisory, student project supervision, designing new programs, research work and administration.

Postdoctoral Research Associate   `9/16-6/17`

CMU USA, Full-time

> Worked as full time research member of Computer Engineering department. Major duties included: literature review, using EDA tools, circuit schematic and layout in advanced technologies, simulation and verification, reporting in research meetings and discussion with graduate students.

Postdoctoral Research Fellow   `3/16-8/2016`

SKKU S. Korea, Full-time

> Worked as full time research member of ISDL Lab at ICT department. Major duties included: literature review, using EDA tools, circuit schematic and layout in advanced technologies, simulation and verification, research article writing & submission, graduate student mentoring, reporting in research meetings and applying for research funding.

Lecturer   `2006-2012`

CIIT Pakistan, Full-time

> Worked as full time lecturer at Electrical and Computer Engineering department. Major responsibilities included: preparing and delivering theory and laboratory courses, designing and evaluating student tasks, student project supervision, conduting and attending hands on workshops for students, and other administrative works as assigned by the chairman.

PATENT ISSUED

- Title: Title: Memory apparatus and method for reading data (메모리 장치 및 판독 방법) Number: 공개특허 10-2019-0031824, Patent issued by Korea IP Rights Information Service Available online at http://engportal.kipris.or.kr/

RESEARCH PROJECTS

- Title: Title: Circuits for Approximate Computing, Funding Agency: DSR-UJ/MOE Saudi Arabia, Amount: 10000 SAR Grant No. UJ-02-009-DR

- Title: Title: Circuits for Low Power operation, Funding Agency: DSR-UJ/MOE Saudi Arabia, Amount: 10000 SAR Grant No. UJ-21-DR-125

- Title: Title: Novel Memory Circuits, Funding Agency: DSR-UJ/MOE Saudi Arabia, Amount: 10000 SAR Grant No. UJ-02-002-DR

COURSES TAUGHT AT UNIVERSITY LEVEL

- Electronics & Circuit Analysis
- Digital Logic Design
- Computer Architecture
- Microprocessors and Microcontrollers
- Embedded Systems
- Computer Networks
- Introduction to Programming
- Data Structures and Algorithms
- Signals and Systems
- Digital Signal Processing
- Digital Communications

RESEARCH PUBLICATIONS (ISI-INDEXED JOURNALS)

1 A. Basit, W. T. Toor, M. Saadi, **N. Maroof**, S. A. Khan, S. Al Otaibi, "Reversible encryption and lossless data hiding for medical imaging aiding smart health care", Cluster Computing (2022), DOI: 10.1007/s10586-022-03792-z

2 MC Parameshwara, **N Maroof**, A Khan, "Majority logic based area-delay efficient 1-bit approximate adder for error-tolerant applications", Engineering Research Express, Vol. 4, No. 2, pp. 025033, DOI: 10.1088/2631-8695/ac7282

3 MC Parameshwara, **N Maroof**, "An Area-Efficient Majority Logic-Based Approximate Adders with Low Delay for Error-Resilient Applications", Circuits Systems and Signal Processing (2022), DOI: 10.1007/s00034-022-02014-6

4 **N. Maroof** and Ali. Y. Al-Zahrani, "A Double bit approximate adder providing a new design perspective", Accepted and pre-published in Journal of Circuits, Systems and Computers, 2021. DOI: 10.1142/S0218126622500657

5 A. Ahmed, K. Park, S.A. Khan, **N. Maroof**, and S. Baeg, "Architectural Design Tradeoffs in SRAM-based TCAMs", IEICE ELEX, vol. 16, no. 13, pp. 20190267, July 2019, DOI: 10.1587/elex.16.20190267

6 W. T. Toor, A. Basit, **N. Maroof**, S. A. Khan, and M. Saadi, "Evolution of random access process: From Legacy networks to 5G and beyond", Transaction on Emerging Telecommunications Technologies, 2019; e3776. DOI: 10.1002/ett.3776

7 A. Basit, S.A. Khan, W.T. Toor, **N. Maroof**, M. Saadi, and A.A. Khan, "A Novel Dissimilarity of Activity Biomarker and Functional Connectivity Analysis for the Epilepsy Diagnosis", Symmetry 2019, vol. 11, no. 8. pp. 979-992, Aug. 2019. DOI: 10.3390/sym11080979

8 **N. Maroof**, and B. S. Kong, "10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage", IEEE Tran. on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 4, pp.1193-1203, April 2017. DOI: 10.1109/TVLSI.2016.2637918

9 **N. Maroof**, and B. S. Kong, "Charge Sharing Write Driver for Low Power SRAM", IET Circuits Systems and Devices, Accepted and online published first, September 2017. DOI: 10.1049/iet-cds.2017.0146

10 **N. Maroof**, M. Sohail, and H. Shin, "Charge sharing read port with bitline pre-charging and sensing scheme for low-power SRAMs", International Journal of Circuit Theory and Applications, Dec. 2016. DOI: 10.1002/cta.2311

11 **N. Maroof**, M. Sohail, and H. Shin, "An energy efficient sub- threshold to above-threshold level shifter using a modified WCM", International Journal of Electronics, vol. 103, no. 7, pp. 1216-1227, July 2016. DOI: 10.1080/00207217.2015.1092596

12 **N. Maroof**, M. Sohail, and H. Shin, "Energy efficient low static- power voltage level shifter", IEICE Electronics Express, vol. 12, no. 18, pp. 20150633, Sept. 2015. DOI: 10.1587/elex.12.20150633

13 **N. Maroof**, M. Sohail, and H. Shin, "Charge sharing based 10T SRAM for low-power", IEICE Electronics Express, vol. 13, no. 5, pp. 20151033, Mar. 2016. DOI: 10.1587/elex.13.20151033

14 **N. Maroof**, M. Sohail, and H. Shin, "A fast and energy efficient two-stage level shifter using controlled WCM", Automatika Journal for Control, Measurement, Electronics, Computing and Communications, vol. 58, no. 4, pp. 473-478, 2017. DOI: 10.1080/00051144.2018.1456099

PROFESSIONAL EXPERTISE

- Embedded System Design
- Integrated Circuit Design
- FPGA based design
- Troubleshooting, VLTI Testing, and IC Reliability
- Teaching and Demonstration
- Curriculum design, review and accreditation
- Lab manuals and lab experiments
- Trainings and seminars
- Student project supervision
- Research, development, testing and documentation
- Technical writing and presentation skills
- Academic writing and publishing
- Research work, Simulations, Data gathering and Analysis

SKILLS

Languages	URDU(native), ENGLISH(fluent), KOREAN(Basic), ARABIC(Basic)
IC Design	Schematic, Layout, DRC, LVS, HSpice, Spectre, Ocean and Skill
EDA Tools	Cadence VIRTUOSO, Mentor Graphics and Synopysys EDA tools
Digital HW	Verilog, HLS, FPGA, ARM embedded boards, Assembly, μ-controllers
Embedded	C/C++, ZEPHYR, RTOS, SENSORS, BLE, CELLULAR, WIFI
Optimization	Variability analysis, Process corner, MC simulations, Matlab, Excel
Software	C/C++, PYTHON, MATLAB
Electronics	AMPLIFIERS, COMPACTORS, ARDUINO, PROTEUS
Editing	MS OFFICE, LaTeX, INKSKAPE

AWARDS / MEMBERSHIPS

○ Full scholarship holder for PhD Engineering in South Korea
○ Full scholarship holder for MSc Engineering in UK
○ Fee-waiver scholarship holder for 4-years BSc Engineering in Pakistan
○ Registered Engineer with Pakistan Engineering council (#***comp/05065***)
○ Registered member of IEEE and IEICE
○ DevZone technical support member
○ Planning to apply for UK HEA Fellowship

REFERENCES

○ Dr. Jamshed M. Iqbal (Ex-Professor of EEE, UJ, KSA),
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